IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
TAILLIET

Serial No. **Not yet assigned**

Filing Date: **Herewith**

For: **METHOD AND SYSTEM FOR THE ADJUSTMENT OF AN INTERNAL TIMING SIGNAL OR A CORRESPONDING REFERENCE IN AN INTEGRATED CIRCUIT, AND CORRESPONDING INTEGRATED CIRCUIT**

I HEREBY CERTIFY THIS PAPER OR FEE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE "EXPRESS MAIL POST OFFICE TO ADDRESSEE" SERVICE UNDER 37 CFR 1.10 ON THE DATE INDICATED BELOW AND IS ADDRESSED TO: BOX PATENT APPLICATIONS, ASSISTANT COMMISSIONER FOR PATENTS, WASHINGTON, D.C. 20231.

EXPRESS MAIL NO: EL 768137828 US
DATE OF DEPOSIT: December 19, 2001
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SIGNATURE: Dawn Kimler

PRELIMINARY AMENDMENT

Director, U.S. Patent and Trademark Office
Washington, D.C. 20231

Sir:

Prior to the calculation of fees and examination of the present application, please enter the amendments and remarks set out below.

In the Drawings:

Submitted herewith is a request for a proposed drawing modification as indicated in red ink to label FIG. 1 as prior art and to translate certain text in FIGS. 1, 2A, 2B and 6 into corresponding English language text. No new matter is being added.

In the Claims:

Please cancel Claims 1 to 24.

Please add new Claims 25 to 60.

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25. A method for adjusting a duration of an internal timing signal in an integrated circuit, the method comprising:

activating the internal timing signal in the integrated circuit;

sequentially sending calibration values to an input of the integrated circuit, the calibration values being based upon a typical value of the duration of the internal timing signal;

determining a last calibration value received or being received by the integrated circuit based upon an expiration of the internal timing signal; and

adjusting the duration of the internal timing signal based upon the determination of the last calibration value.

26. The method according to Claim 25 wherein each calibration value corresponds to a ratio of the typical value to a total duration that has elapsed from activation of the internal timing signal to a time when the calibration value is sent.

27. The method according to Claim 26 wherein the adjusting is performed by an adjustment device including an initialization value.

28. The method according to Claim 27 further comprising assigning a factor to each calibration value corresponding to the initialization value.

29. The method according to Claim 25 wherein sequentially sending the calibration values comprises

sequentially sending the calibration values after a predetermined period has elapsed.

30. The method according to Claim 25 wherein the internal timing signal is a function of at least one reference provided by a reference circuit, and wherein adjusting the duration of the internal timing signal comprises adjusting the duration of the internal timing signal via the reference circuit.

31. A method for adjusting a reference in at least one integrated circuit comprising:

generating an internal timing signal in the at least one integrated circuit based upon the reference;

adjusting a duration of the internal timing signal to obtain calibration data; and

adjusting the reference in the at least one integrated circuit based upon the calibration data.

32. The method of Claim 31 wherein adjusting the reference comprises adjusting the reference using a reference circuit in the at least one integrated circuit.

33. The method of Claim 32 wherein the reference circuit comprises a current source.

34. The method of Claim 32 wherein the reference circuit comprises at least one capacitor.

35. The method of Claim 32 wherein the calibration data is also applied to a reference circuit of at least one additional integrated circuit, the reference circuit of the at least one additional integrated circuit being substantially

identical to the reference circuit of the at least one integrated circuit.

36. The method of Claim 31 wherein the at least one integrated circuit comprises a non-volatile memory integrated circuit, and wherein the reference comprises a signal for programming the non-volatile memory integrated circuit.

37. The method of Claim 36 wherein adjusting the duration of the internal timing signal comprises:

programming data at an address in the non-volatile memory integrated circuit; and

successively sending calibration values to an input of the integrated circuit to determine an end of the programming based upon a last calibration value received or being received.

38. The method of Claim 37 further comprising sending all of the calibration values to the non-volatile memory integrated circuit prior to programming, and wherein the calibration values are defined as a function of specifications of the non-volatile memory integrated circuit.

39. The method of Claim 37 wherein the address is determined internally to the integrated circuit.

40. The method of Claim 37 wherein programming data at the address comprises programming data based upon an external programming command.

41. The method of Claim 37 wherein the non-volatile memory integrated circuit further comprises a data input

register, and wherein the calibration values are stored in the data input register.

42. A method for adjusting respective references in a plurality of integrated circuits comprising:

generating an internal timing signal in a first one of the integrated circuits based upon the reference thereof;

adjusting a duration of the internal timing signal to obtain calibration data; and

adjusting the reference in each of the integrated circuits using respective reference circuits thereof based upon the calibration data.

43. The method of Claim 42 wherein the reference circuit comprises a current source.

44. The method of Claim 42 wherein the reference circuit comprises at least one capacitor.

45. The method of Claim 42 wherein the reference circuits of the integrated circuits are substantially identical to one another.

46. The method of Claim 42 wherein the reference comprises a signal for programming the memory.

47. The method of Claim 46 wherein the integrated circuits comprises non-volatile memory integrated circuits, and wherein adjusting the duration of the internal timing signal comprises:

programming data at an address in the first non-volatile memory integrated circuit; and

successively sending calibration values to an input of the first non-volatile memory integrated circuit to determine an end of the programming based upon a last calibration value received or being received.

48. The method of Claim 47 further comprising sending all of the calibration values to the first non-volatile memory integrated circuit prior to programming, and wherein the calibration values are defined as a function of specifications of the non-volatile memory integrated circuit.

49. The method of Claim 47 wherein the address is determined internally to the integrated circuit.

50. The method of Claim 47 wherein programming data at the address comprises programming data based upon an external programming command.

51. The method of Claim 47 wherein the first non-volatile memory integrated circuit further comprises a data input register, and wherein the calibration values are stored in the data input register.

52. An integrated circuit comprising:

a circuit for generating an internal timing signal from at least one reference;

temporary storage means for recording data sent to a data input of the integrated circuit after an activation of the internal timing signal;

a non-volatile memory element for storing data present in said temporary storage means upon an expiration of the internal timing signal; and

a reference circuit and at least one adjustment device associated therewith for cooperating to adjust the at least one reference based upon the data stored in said non-volatile memory element.

53. The integrated circuit according to Claim 52 wherein said reference circuit comprises a plurality of reference circuits, and a first one of said reference circuits being associated with said internal timing signal generating circuit; and wherein said at least one adjustment device comprises a first adjustment device for adjusting the first reference circuit and at least one second adjustment device for adjusting another of said reference circuits, said other reference circuit being substantially identical to said first reference circuit, and the data stored in said non-volatile memory element being applied to said first and second adjustment devices.

54. The integrated circuit according to Claim 52 wherein the integrated circuit comprises a non-volatile memory device, wherein the internal timing signal comprises a programming signal for the non-volatile memory, and wherein said temporary storage means comprises a data input register.

55. The integrated circuit according to Claim 52 wherein said reference circuit comprises a current reference circuit.

56. The integrated circuit according to Claim 52 wherein said reference circuit comprises at least one of a capacitor and a capacitor network.

57. The integrated circuit according to Claim 52 wherein said reference circuit comprises at least one resistor.

58. An integrated circuit comprising:

an array of non-volatile memory cells;

a circuit for generating an internal timing signal from at least one reference, the internal timing signal being a programming signal for the non-volatile memory cells;

a temporary storage device for recording data sent to at least one data input of the integrated circuit after an activation of the internal timing signal;

said array of non-volatile memory cells comprising at least one cell for storing data present in said temporary storage device upon an expiration of the internal timing signal; and

a reference circuit and at least one adjustment device associated therewith for cooperating to adjust the at least one reference based upon the data stored in said at least one cell.

59. The integrated circuit according to Claim 58 wherein said reference circuit comprises a plurality of reference circuits and a first one of said reference circuits being associated with said internal timing signal generating circuit; and wherein said at least one adjustment device comprises a first adjustment device for adjusting the first reference circuit and at least one second adjustment device for adjusting another of said reference circuits, said other reference circuit being substantially identical to said first reference circuit, and the data stored in said at least one cell being applied to said first and second adjustment

devices.

60. The integrated circuit according to Claim 58 wherein said reference circuit comprises at least one of a current reference circuit, a capacitor, and a resistor network.

REMARKS

It is believed that all of the claims are patentable over the prior art. For better readability and the Examiner=s convenience, the newly submitted claims differ from the translated counterpart claims which are being canceled. The newly submitted claims do not represent changes or amendments that narrow the claim scope for any reason related to the statutory requirements for patentability. Accordingly, after the Examiner completes a thorough examination and finds the claims patentable, a Notice of Allowance is respectfully requested in due course. Should the Examiner determine any minor informalities that need to be addressed, he is encouraged to contact the undersigned attorney at the telephone number below.

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Respectfully submitted,

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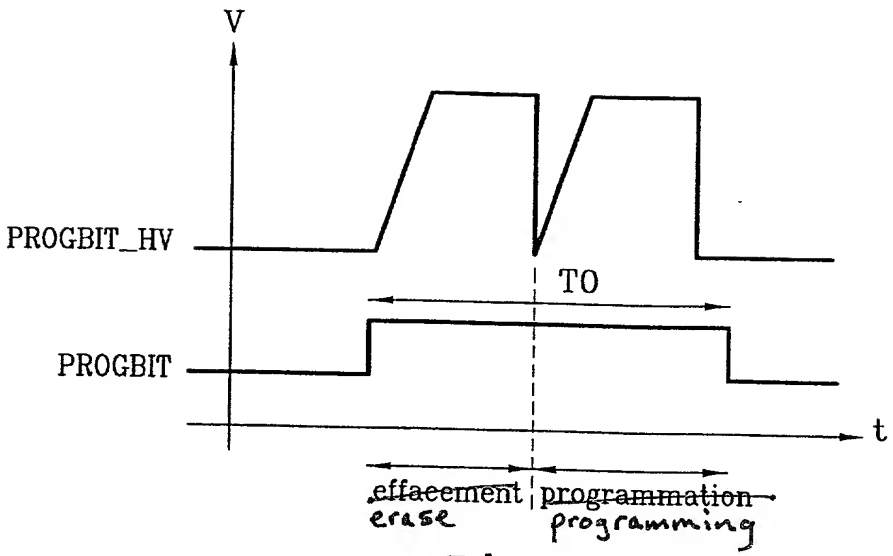


Fig. 1
(PRIOR ART)

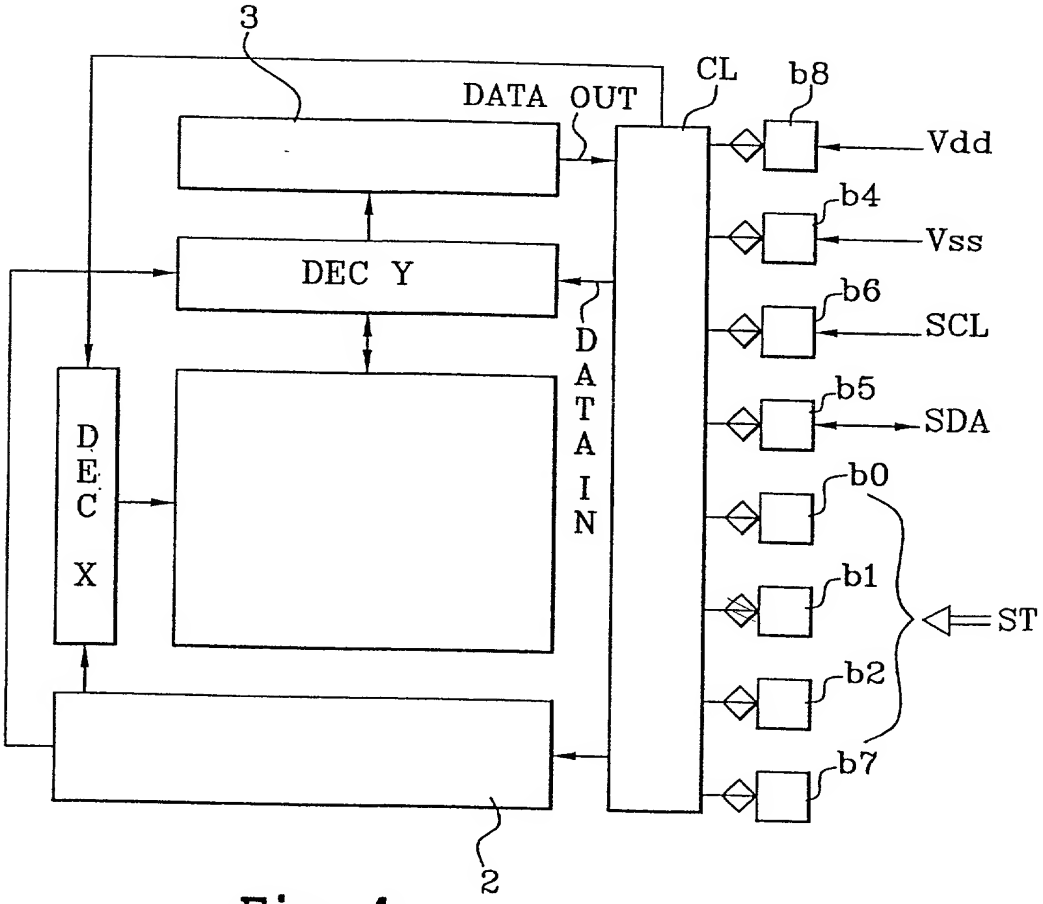


Fig. 4

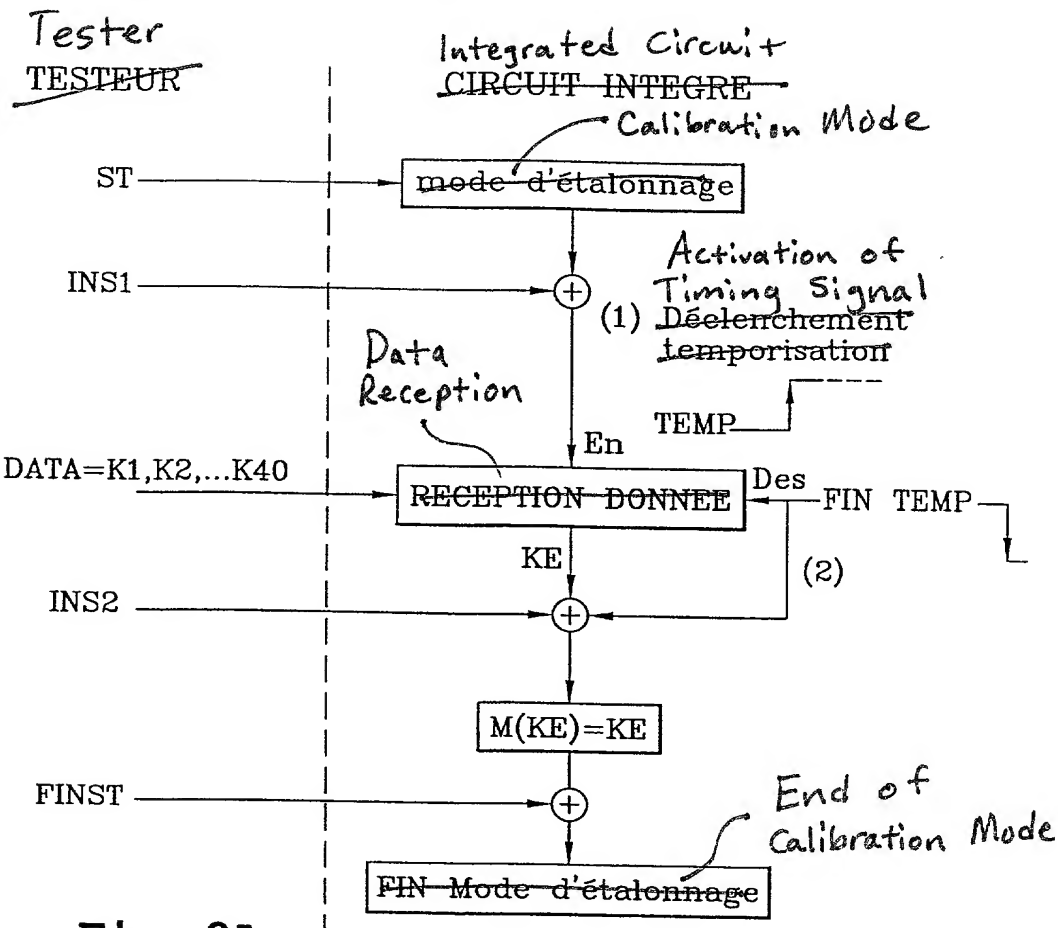
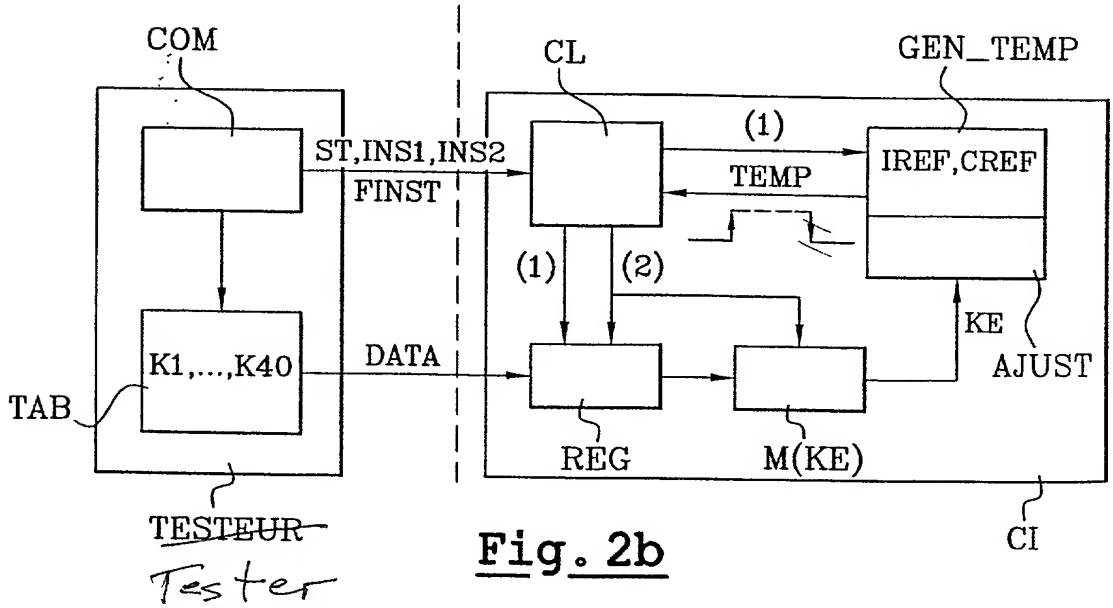

Tester
TESTEUR
Integrated Circuit
CIRCUIT INTEGRE
Calibration Mode
ST
mode d'étalonnage
INS1
Activation of Timing Signal
(1) Déclenchement temporisation
Data Reception
TEMP
En
DATA=K1,K2,...K40
RECEPTION DONNEE
Des
FIN TEMP
KE
(2)
INS2
M(KE)=KE
FINST
End of Calibration Mode
FIN Mode d'étalonnage

Fig. 2A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CL
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(1)
TEMP
IREF,CREF
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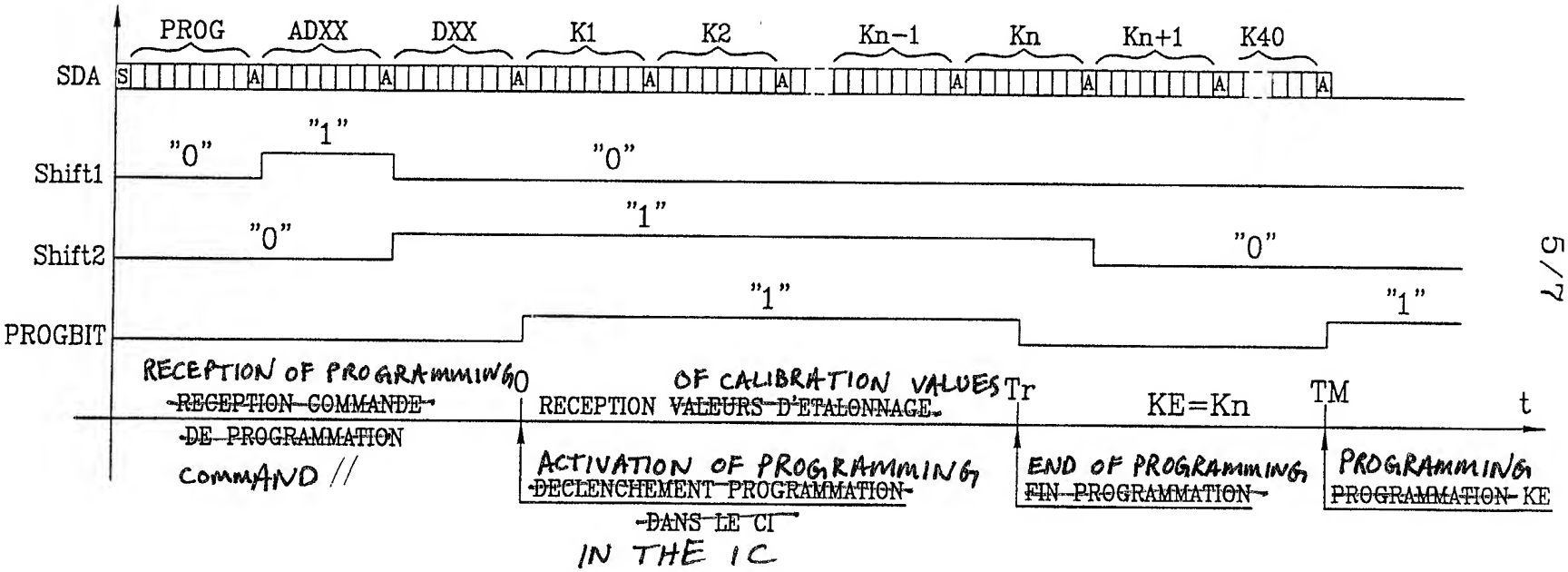
K1,...,K40
DATA
AJUST
TAB
REG
M(KE)
TESTEUR
Tester
CI

Fig. 2b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DXX
K1
K2
Kn-1
Kn
Kn+1
K40
SDA
S
A
Shift1
Shift2
PROGBIT
"0"
"1"
RECEPTION OF PROGRAMMING COMMAND //
RECEPTION OF CALIBRATION VALUES
ACTIVATION OF PROGRAMMING IN THE IC
END OF PROGRAMMING
PROGRAMMING KE
0
Tr
KE=Kn
TM
t

Fig. 6